Amendments to the Drawings:

The attached nine sheets of drawings include FIGS. 1-6. These sheets replace the original sheet including FIGS. 1-6. The submission of replacement sheets is in response to the Form PTO-948 dated August 17, 2006.

FIG. 1 is now presented as FIGS. 1A through 1E. FIG. 2 is now presented as FIGS. 2A through 2F. In FIG. 3B, the lines on the graph have been patterned to readily identify each without requiring reference to the specification. FIG. 5 is now presented as FIGS. 5A through 5J. The text-steps that appeared in the original FIG. 5 have been moved into the specification. FIG. 6 is now presented as FIGS. 6A and 6B. A label "Emitted light 311" which originally appeared in the "B" portion of the original FIG. 6, is added in FIG. 6A.

No new matter is added.

Attachment: Replacement Sheets

Annotated Sheets Showing Changes

REMARKS

Claims 1-18, 25-32, and 39-48 are all the claims pending in the application. These claims were allowed in a Notice of Allowance dated May 25, 2006.

Claim 32 is amended to delete an extraneous "a" left over after the previous amendment. As all claims have been allowed, the "withdrawn" identifiers have been removed from the claims.

In response to the Notice Regarding Drawings mailed August 17, 2006, this Amendment includes a substitute specification making the following changes:

- The text is adjusted for the new numbering of the claims.
- The steps that were originally enumerated on the face of FIG. 5 have been imported into the specification and deleted from the drawings.

Steps 34 and 35 from original FIG. 5 were not explicitly referenced in the text of the original specification. These steps have been included under the newly added label of "Finishing" in paragraph 0029 of the substitute specification. In context, it is not believed that "Finishing" constitutes new matter.

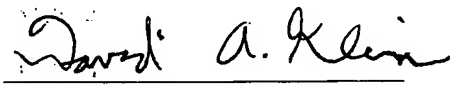
Also in the original FIG. 5, several steps appeared in bold and underline with a chain of dots leading to the adjacent figure. In the substitute specification, those steps are now called out with a reference (*e.g.*, "see FIG. 5A") to the corresponding figure in the Replacement Drawings.

None of the changes in the substitute specification and drawings are believed to constitute new matter. Entry and consideration are requested.

Applicants authorize the Commissioner to charge any fees determined to be due with the exception of the issue fee and to credit any overpayment to Deposit Account No. 11-0600.

The Examiner is invited to contact the undersigned at (202) 220-4209 to discuss any matter concerning this application.

Respectfully submitted,
KENYON & KENYON LLP



David A. Klein
Reg. No. 46,835

Dated: August 25, 2006

Kenyon & Kenyon LLP
1500 K Street, N.W.
Suite 700
Washington, D.C. 20005
Tel: (202) 220-4200
Fax: (202) 220-4201

SUBSTITUTE SPECIFICATION (WITH MARKINGS)

METHOD OF FABRICATION OF A SUPPORT STRUCTURE FOR A SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

[0001] This application claims priority to U.S. Provisional Application 60/434,671 filed on December 20, 2002.

[0002] The present invention pertains to the fabrication of a semiconductor device or an integrated circuit (IC). More particularly, the present invention pertains to the fabrication of a device or IC through the extensive growth of a semiconductor layer of a desired doping profile and defect density on a conventional wafer.

[0003] Electronic devices and integrated circuits, and methods for their fabrication, are well known in the art. Typically, the fabrication process starts with a semiconductor substrate with a suitable doping level and defect density. The elements of the device or circuit are then formed on or just below the surface of the substrate through additive processes (such as material deposition using such techniques as chemical vapor deposition (CVD) or sputtering), subtractive processes (such as etching) or processes that modify the properties of the existing material (such as ion implantation or thermal annealing). The processes can be performed selectively using well-known photolithographic techniques to form masking layers on the substrate surface.

[0004] One example of an electronic device that can be formed using such processes is a surface emitting laser.

[0005] In general, the performance of an electronic device depends not only upon the structure grown or formed on the substrate surface, but also upon the properties of the substrate itself. For example, the doping level in the substrate may affect series resistance and current density distribution if the current flows through the substrate, junction capacitance for junction isolated devices, or latch-up tolerance in devices with parasitic thyristors (such as CMOS ICs). Defect densities are also important, affecting leakage currents and device reliability. In the case of an

optical device emitting through the substrate (such as a NECSEL (Novalux® Extended Cavity Surface Emitting Laser)), optical absorption in the substrate is also important.

[0006] In the particular case of a NECSEL or bottom emitting VCSEL (Vertical Cavity Surface Emitting Laser), the importance of the substrate properties is as follows. The current flowing to the gain region passes through the substrate. High conductivity is required to keep the series resistance low and prevent too much current crowding at the device perimeter. This can be achieved through the use of a heavily doped, thick substrate. On the other hand, optical loss must be kept low and this means a low doping level and thin substrate. A third requirement arises from the need to maintain device operation within specification over its entire lifetime. A key element in achieving this is to keep the defect density in the substrate low. An acceptable trade-off between these three requirements (low resistance, low optical loss and low defect density) is difficult to achieve in commercially available substrate materials.

[0007] In view of this, there is a need for an improved method of manufacture of an electronic device or integrated circuit that eliminates the need for the starting substrate to meet all three of the requirements noted above.

SUMMARY OF THE INVENTION

[0008] According to an embodiment of the present invention, a method of fabricating a semiconductor device is described. In this method, a starting substrate of sufficient thickness is selected that has the required (usually low) defect density. Normal methods of substrate growth, such as the VGF (vertical gradient freeze) technique, can only achieve low defect densities if the doping level is high (greater than 1×10^{18} cm^{-3} in GaAs, for example). Such high doping levels are usually undesirable for bottom emitting VCSELs or NECSELs as described above. However, according to the present invention, a highly doped low defect density substrate can be used as the starting material. A semiconductor layer is epitaxially grown on top of the low defect density starting material. The grown material can be any material that can be grown with high crystal quality on the starting material. Typically it will be the same as the starting material (for example, GaAs on GaAs) but other material combinations are possible (for example AlGaAsP on GaAs where the AlGaAsP composition is adjusted to give a close lattice match with the underlying GaAs). Any suitable epitaxial growth technique can be used for the semiconductor

layer (including MOCVD, MBE, etc). If the growth conditions are correctly chosen, the crystal quality (including defect density) will match or be better than that of the underlying material.

[0009] The active components, electrical contacts etc. are formed on top of the grown semiconductor layer using well-established wafer-scale fabrication techniques. At an appropriate stage during this fabrication, the original substrate material is removed from the whole wafer by any suitable technique (mechanical polishing, chemical etching, chemical-mechanical polishing (CMP), chemical or physical plasma etching etc.) leaving only a sufficient thickness of the grown semiconductor layer to provide mechanical support for the active components once they are separated into individual die. Typically, the thinning of the wafer will be performed at or close to the end of the active device fabrication sequence so that the thicker starting material is present to provide mechanical support during most or all of the wafer fabrication sequence.

[0010] In one embodiment of the invention, the doping of the grown semiconductor layer is uniform and can be selected for optimum device performance. Low defect density is achieved as described above and is fully decoupled from the doping density. In a second embodiment, the doping density is not uniform. For example, it might be kept very low (less than 1×10^{16} cm^{-3}) through most of the grown layer to minimize optical absorption and increased only in a thin region close to the active devices to provide good electrical conduction.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] ~~FIG. 1~~FIGS. 1A-1E are diagrams presenting a fabrication process for a NECSEL semiconductor device as is known in the art.

[0012] ~~FIG. 2~~FIGS. 2A-2F are diagrams presenting a fabrication process for a semiconductor device according to an embodiment of the present invention.

[0013] FIGS. ~~3a-b~~3A and 3B are graphs showing wall plug efficiency (WPE) for NECSEL devices incorporating the semiconductor layer of FIG. 2 built according to embodiments of the present invention.

[0014] FIG. 4 is a flow chart of a semiconductor fabrication process according to an embodiment of the present invention.

[0015] ~~FIG. 5~~FIGS. 5A-5J ~~depicts~~ depict a fabrication process for an optical device using the semiconductor layer of FIG. 2.

[0016] ~~FIG. 6 depicts~~FIGS. 6A and 6B depict a completed optical semiconductor device (e.g., a NECSEL), built according to an embodiment of the present invention.

DETAILED DESCRIPTION

[0017] Referring to ~~FIG. 1~~FIGS. 1A through 1E, an example of a semiconductor fabrication process is presented for an optical device, in this case a NECSEL, as it is known in the art. In this example, the starting substrate 101 is a low-doped 4-inch GaAs wafer. In the second diagram, the device layer, 103, is grown epitaxially on one surface of the wafer. In the case of a NECSEL, the device layer includes distributed Bragg reflectors (DBRs) and quantum wells to provide optical gain. In the third diagram, the NECSEL device is further fabricated, and electrical contacts 105 are added. In the fourth diagram the substrate is thinned to the desired final thickness and polished to give the necessary optical quality finish. In the fifth diagram, an anti-reflective coating (ARC), 106, and an optical aperture, 107, are formed on the polished surface to complete the NECSEL die. In operation, light is generated in the device and is emitted as shown by the large arrow.

[0018] Referring to ~~FIG. 2~~FIGS. 2A through 2F, an example of a semiconductor fabrication process for an optical device is presented according to an embodiment of the present invention. In this embodiment, wafer 111 is selected to meet the defect density requirements of the optical device without regard to doping density. Suitable GaAs wafers with low defect densities (etch-pit density, or EPD, values of less than $500cm^{-2}$) are readily available from manufacturers but typically have doping levels of approximately 1×10^{18} cm^{-3} or higher. Such material is commonly grown using a well-known VGF (vertical gradient freeze) technique. The high doping level typically renders them unsuitable for NECSELs. A GaAs layer, 112, is then grown on the starting substrate. The thickness of this layer is selected to provide sufficient mechanical support for the final devices while the doping level (uniform or non-uniform) is selected for optimum laser performance. With proper selection of growth conditions, the defect density in the grown layer will be similar to or better than that of the starting substrate. Once the high-quality support layer, 112, is grown, the rest of the device fabrication may proceed as shown in

FIG. 1. The device layer 113 is grown, and the NECSEL device is fabricated with electrical contacts 115. A key element of the present invention, however, is that the wafer thinning step now removes all of the starting substrate 111. In this way, when the device is completed, with anti-reflective coating (ARC), 116, and an optical aperture, 117, none of the original substrate remains. It is thus possible to combine arbitrary doping profiles (including very low dopant density) with the low defect density normally requiring high dopant density.

[0019] According to a first embodiment of the present invention, the support layer 112 has a uniform doping level of between 5 x 10^{16} cm^{-3} and 5 x 10^{17} cm^{-3} and a thickness of about 100μm.

[0020] According to a second embodiment of the present invention, the support layer 112 is doped very lightly through most of the material (for example, less than 1 x 10^{16} cm^{-3}) in order to minimize optical absorption, while a thin (e.g., 2 to 20μm thick) layer of more heavily doped material (for example, 5 x 10^{17} cm^{-3} and 5 x 10^{18} cm^{-3}) is formed immediately adjacent to the device layer to provide electrical conduction. Such a tailored doping profile is readily obtained, for example, by adjusting dopant source flow rates during epitaxial growth by metal organic chemical vapor deposition (MOCVD).

[0021] The effect of tailoring the doping profile in this way can be described in more detail with respect to FIGS. ~~3a-b~~3A and 3B. The figures show the modeled wall plug efficiency (WPE) for various NECSEL designs. The wall plug efficiency is the ratio of the optical power emitted by the NECSEL to the input electrical power and is an important performance value for diode lasers. In general, high wall plug efficiency is desired. FIG. ~~3a~~ 3A illustrates what can be achieved with a uniform substrate doping by changing that doping level. For the sake of this example, a NECSEL diameter of 80μm and a substrate thickness of 100μm are assumed. The peak WPE is about 10% and is achieved with a uniform substrate doping of about 2 x 10^{17} cm^{-2}. From the point of view of maximizing WPE, this substrate doping represents the best compromise between low series resistance and low optical absorption.

[0022] FIG. ~~3b~~3B, however, shows that better performance can be achieved by using a tailored substrate doping profile. In this case, most of the grown support substrate is doped to 1 x 10^{16} cm^{-3}, but a thin shunt layer (having a thickness between 0 and 10μm) of more heavily doped material is added adjacent to the device layer as described above. Three n-type doping levels are considered in the shunt layer: 2 x 10^{17} cm^{-3}, 5 x 10^{17} cm^{-3}, and 1 x 10^{18} cm^{-3}. The three curves show the variation in WPE as the shunt layer thickness is adjusted: curve 200a shows simulated

results for a shunt doping of 2 x 10^{17} cm^{-3}, curve 200b shows results for a shunt doping of 5 x 10^{17} cm^{-3}, and curve 200c shows results for a shunt doping of 1 x 10^{18} cm^{-3}. It is clear that with the two higher shunt doping levels, higher WPE values can be achieved with the tailored substrate doping design than can be achieved using a uniformly doped substrate. For example, with a shunt doping of 1 x 10^{18} cm^{-3} and a shunt thickness of about 8μm, the peak WPE is about 12%.

[0023] The calculations discussed above show that embodiments of the present invention offer not only improved reliability (through lower substrate defect density) but also better device performance. The calculations are based on one example of a NECSEL design. However, tailoring the substrate doping profile can be applied to other NECSEL and optical device designs with different device diameters, substrate thicknesses, or device layer designs. The specific optimum doping profile (shunt thickness and doping level) will in general be different for different optical device designs.

[0024] An example of an overall process sequence for fabricating a semiconductor device according to an embodiment of the present invention is summarized with reference to FIG. 4. In block 121 of the flow diagram a starting substrate is selected. As discussed above, the starting substrate may be selected on the basis of defect density alone without regard for doping level or even dopant type. In block 123 a semiconductor layer having a desired thickness is disposed onto the starting substrate with a desired doping profile. In the examples discussed above, the semiconductor layer might have a uniform doping of between 5 x 10^{16} cm^{-3} and 5 x 10^{17} cm^{-3} or may have a more complex doping profile with two or more doping levels at different depths and selected gradients between those levels. The material of the semiconductor layer should either be the same as the starting substrate (for example, GaAs grown on GaAs) or be of a composition such that it can be grown epitaxially with good crystal quality (for example, AlGaAsP grown on GaAs where the AlGaAsP composition is selected to give a good lattice match to the GaAs). In block 125, optional refinishing of the wafer surface can be performed in preparation for growth of the active device layer. In block 127, the active layer(s) required for the intended devices are grown. For example, for a NECSEL appropriate distributed Bragg reflectors (DBRs) and quantum wells are grown. In block 129 the processing required to form the active devices is carried out using known techniques such as dielectric and metal deposition, photolithography, etching, implantation and annealing. In block 131 the original starting substrate is completely

removed using a technique such as, for example, mechanical or chemical-mechanical polishing or chemical etching. Finally in block 133, any additional layers or structures required on the opposite side of the substrate are formed, again using known techniques. The devices on the wafer are then complete. The wafer can be separated into individual die and those dice mounted and electrical contacts made using well-known methods.

[0025] Several techniques for removing the starting substrate material can be applied in order to implement embodiments of the current invention. In one embodiment, mechanical or chemical-mechanical polishing is used to remove the material. In the embodiment described above, the grown material and starting substrate material are very similar (both are GaAs and they differ only in the doping level). It is thus difficult to determine exactly when the original starting material is fully removed. This is overcome by growing more material in layer 112 than is needed in the final device, and removing some of the grown layer (for example, 10 to 20μm) with the substrate. The polishing process can be timed or the wafer thickness measured in order to ensure full removal of the substrate.

[0026] An alternative embodiment uses a chemical etch to remove the starting substrate. A suitable etch stop is grown on the starting substrate before growth of the support layer 112. Examples of suitable etch-stop layers include AlGaAs and GaAsP. In the case of an AlGaAs etch-stop, the GaAs substrate could be removed with, for example, a citric acid / hydrogen peroxide / water mixture that etches GaAs preferentially over AlGaAs. With a GaAsP etch-stop, an example of a suitable etch is ammonium hydroxide / hydrogen peroxide / water. Once the starting substrate is removed, the etch stop layer can either be left in place or removed by a further chemical etch.

[0027] It is also possible to combine the substrate removal processes discussed above. For example, polishing could be used to remove most of the starting GaAs with chemical etching used to remove the remaining material and finish accurately on the etch-stop.

[0028] Embodiments of the present invention are based on epitaxial growth of single crystal material on a semiconductor substrate. The various embodiments can be realized using any suitable method for epitaxial growth, including, but not limited to, metal organic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE), vapor phase epitaxy (VPE) or liquid phase epitaxy (LPE).

[0029] An example of the fabrication of a semiconductor device using the present invention is described with reference to ~~FIG. 5~~FIGS. 5A through 5J. The first figure shows a cross section of the wafer after epitaxial growth, including the support semiconductor layer and the device active layer. The fabrication process combines known semiconductor processing steps as follows to form the NECSEL die:

a. Creation of fiducial marks used to align the masks defining the patterns for subsequent layers (steps 1-3).

   Step 1. Starting wafer after epitaxial growth (see FIG. 5A).

   Step 2. Photolith 1: Fiducial mask (for subsequent alignment).

   Step 3. Fiducial metal deposition and lift-off (not shown).

b. Current confinement (steps 4-8). This is achieved using a proton implant that reduces the conductivity of the p-DBR outside the required gain aperture by about a factor of about 10,000. The NECSEL will still function without this implant, but current flows outside the gain aperture, reducing wall-plug efficiency. A sacrificial nitride layer covers the wafer during this entire process. The high-energy implant easily penetrates through this layer, and removal of the layer ensures that any contaminants from the implantation or masking steps do not remain on the wafer.

   Step 4. Nitride deposition.

   Step 5. Photolith 2: Resist mask for implant.

   Step 6. Proton implant (see FIG. 5B).

   Step 7. Resist strip.

   Step 8. Nitride removal.

c. Separation of the epitaxial layer into isolated mesas (steps 9-11). This not only allows electrical contact to the substrate layer but also alleviates the strain inherent in the epitaxial layer, flattening the final die for improved die attach, more consistent performance and better reliability.

   Step 9. Photolith 3: Mesa mask.

   Step 10. Etch mesas (see FIG. 5C).

   Step 11. Resist strip.

d. Wafer passivation (steps 12-15). A nitride layer passivates the wafer surface and mesa sidewalls; vias are opened in the nitride for electrical contacts.

Step 12. Nitride deposition.

Step 13. Photolith 4: nitride.

Step 14. Nitride etch (see FIG. 5D).

Step 15. Resist strip.

e. Creation of electrical contacts to the anode and cathode of the laser diode (steps 16-26). The contacts are formed on the same side of the die to enable a robust and reliable die attach process once wafer processing is complete.

Step 16. Photolith 5: P-metal lift-off mask.

Step 17. P-metal stack deposition.

Step 18. P-metal lift-off (see FIG. 5E).

Step 19. P-metal sinter.

Step 20. Photolith 6: N-metal lift-off mask.

Step 21. N-metal stack deposition.

Step 22. N-metal lift-off (see FIG. 5F).

Step 23. N-metal sinter.

Step 24. Photolith 7: First metal lift-off mask.

Step 25. First metal deposition.

Step 26. First metal lift-off (see FIG. 5G).

f. On-wafer test (step 27). Full laser operation can be checked at this early stage in manufacturing.

Step 27. On-wafer test.

g. Wafer thinning to remove the starting substrate material. (steps 28-29).

Step 28. Wafer mount (epi side down) on sapphire substrate.

Step 29. Wafer thinning (lap and polish) (see FIG. 5H).

h. Formation of an anti-reflecting layer on the output surface, essential for good mode control and smooth L-I characteristics in the final product (step 30).

Step 30. Anti-reflection coating (ARC) deposition (see FIG. 5I).

i. Formation of an optical aperture on the output surface to improve mode control (steps 31-33). The aperture is defined using a metal layer.

Step 31. Photolith 8: Aperature metal lift-off mask.

Step 32. Aperture metal deposition.

Step 33. Aperture metal lift-off (see FIG. 5J).

j. Finishing (steps 34-35).

Step 34. De-mount from sapphire substrate.

Step 35. Scribe and break.

[0030] The structure of the completed NECSEL is described with reference to FIG. 6. The NECSEL die, 301, including epitaxial layer 303 is fabricated as described above. The die is soldered to the sub-mount / heat spreader 305 using known techniques. The laser is completed using an external mirror 307 to form an external cavity 309. This structure is described in the art (US patents 6,243,407 and 6,404,797, the disclosure of which are hereby incorporated by reference in their entirety).

[0031] Although the NECSEL fabrication sequence is used here for illustration, the present invention can also be used to build other types of semiconductor devices.

Fig. 1

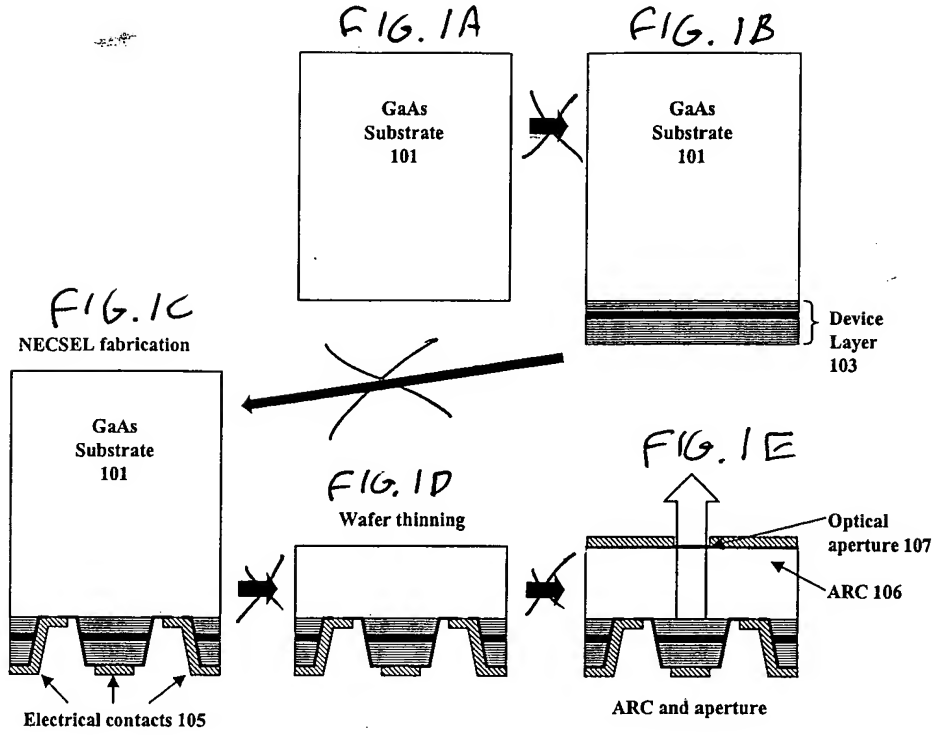
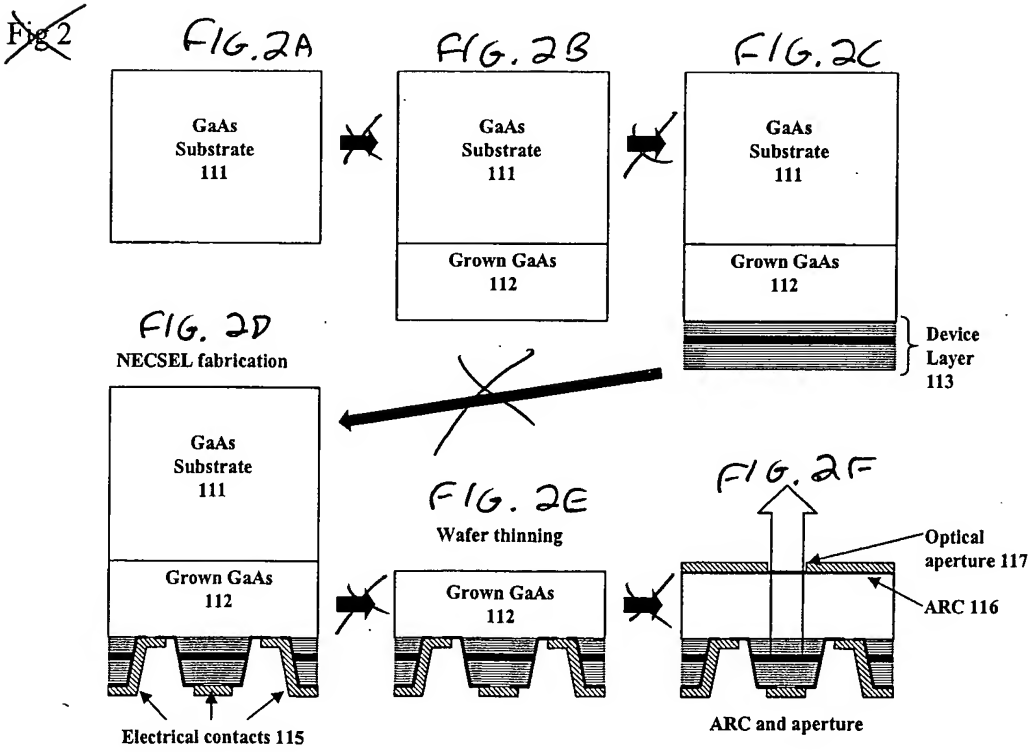


Fig 2



Annotated Marked-Up Drawing
Serial No. 10/735,695 Filed: 12/16/2003
Title: Method of Fabrication of a Support Structure For A Semiconductor Device
Glen Carey et al. Dkt No. 11809/27

Fig 3a

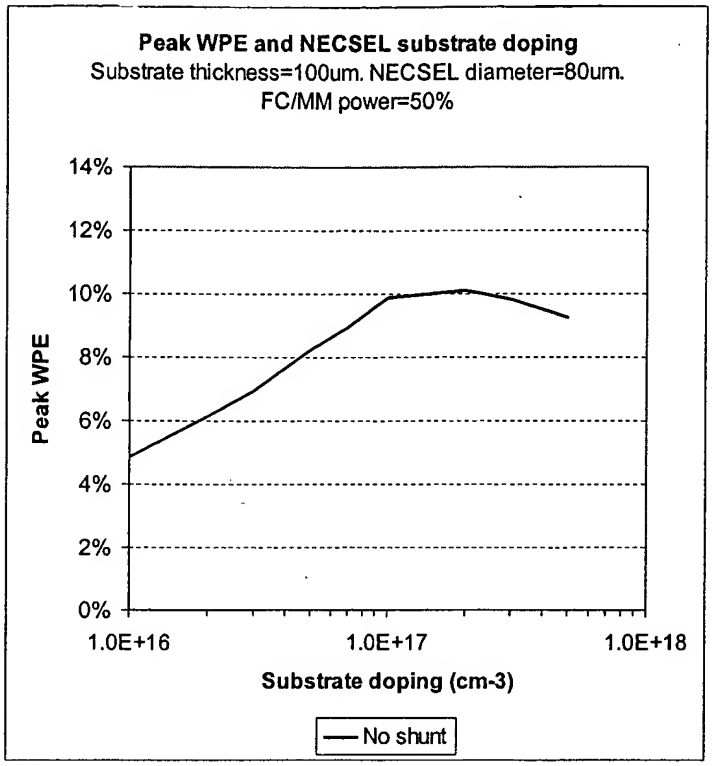


Fig 3b

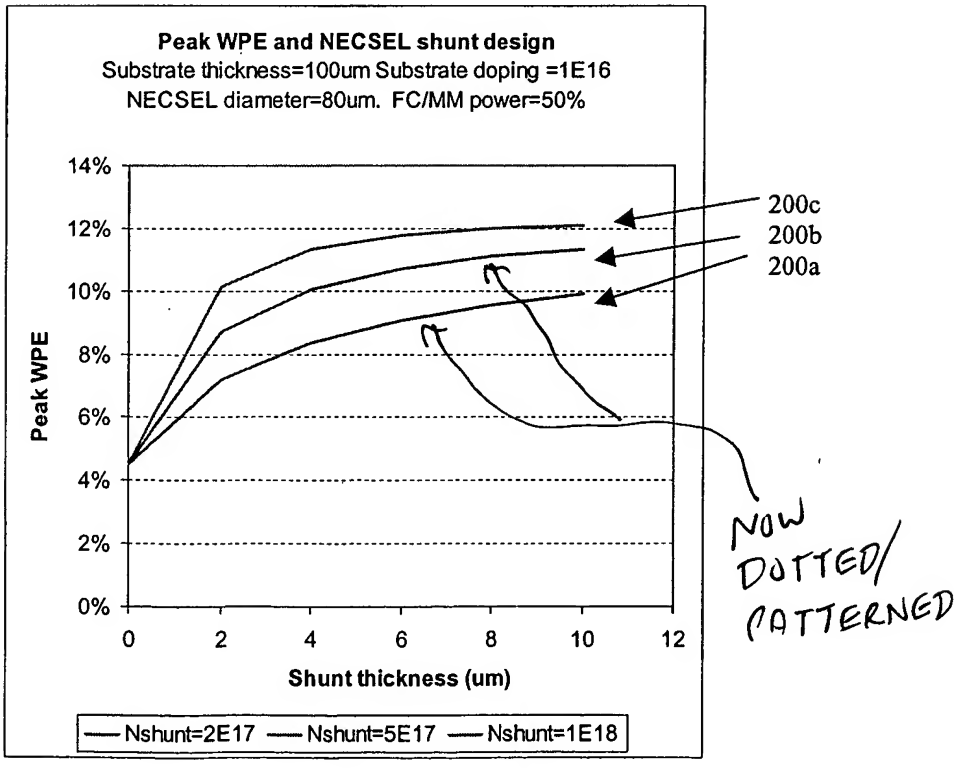
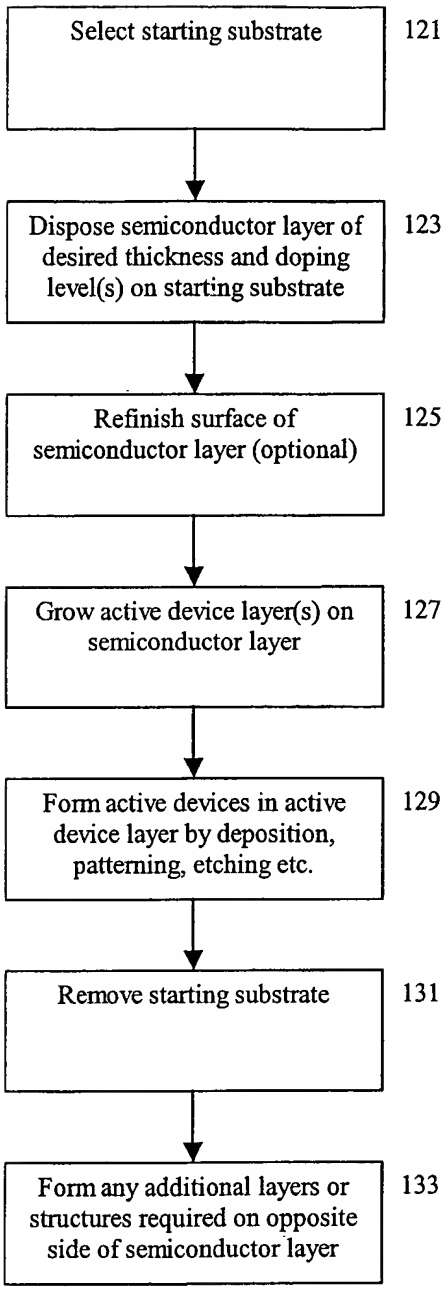


Fig. 4


Select starting substrate
121
Dispose semiconductor layer of desired thickness and doping level(s) on starting substrate
123
Refinish surface of semiconductor layer (optional)
125
Grow active device layer(s) on semiconductor layer
127
Form active devices in active device layer by deposition, patterning, etching etc.
129
Remove starting substrate
131
Form any additional layers or structures required on opposite side of semiconductor layer
133

Annotated Marked-Up Drawing
Serial No. 10/735,695 Filed: 12/16/2003
Title: Method of Fabrication of a Support Structure For A Semiconductor Device
Glen Carey et al. Dkt No. 11809/27

Fig 5.

MOVED TO SPEC

1. **Starting wafer after epitaxial growth**.....

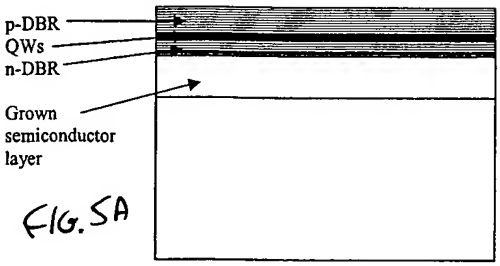


FIG. 5A

2. Photolith 1: Fiducial mask (for subsequent alignment)
3. Fiducial metal deposition and lift-off (not shown)
4. Nitride deposition
5. Photolith 2: Resist mask for implant
6. **Proton implant**.....
7. Resist strip
8. Nitride removal

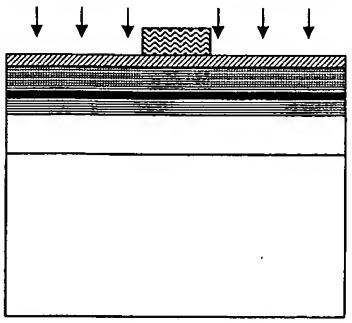


FIG. 5B

9. Photolith 3: Mesa mask
10. **Etch mesas**.....
11. Resist strip

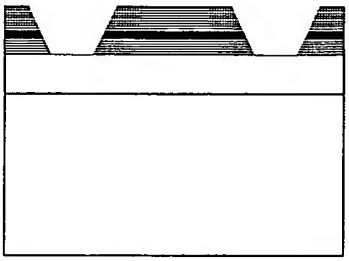


FIG. 5C

12. Nitride deposition
13. Photolith 4: nitride
14. **Nitride etch**.....
15. Resist strip

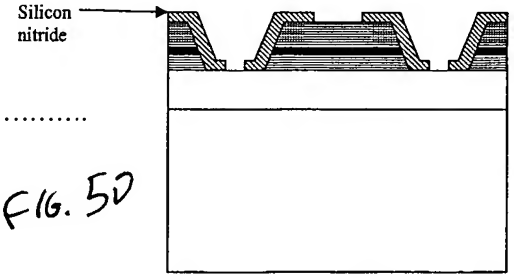


FIG. 5D

16. Photolith 5: P-metal lift-off mask
17. P-metal stack deposition
18. **P-metal lift-off**.....
19. P-metal sinter

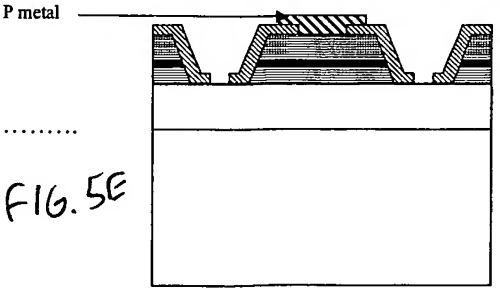
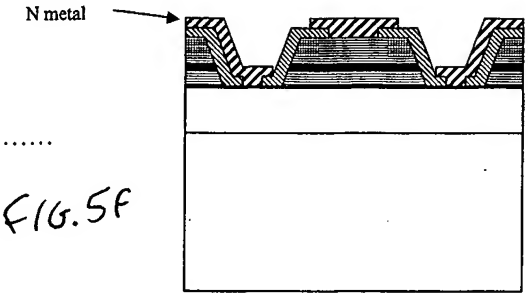


FIG. 5E

Annotated Marked-Up Drawing
Serial No. 10/735,695 Filed: 12/16/2003
Title: Method of Fabrication of a Support Structure For A Semiconductor Device
Glen Carey et al. Dkt No. 11809/27

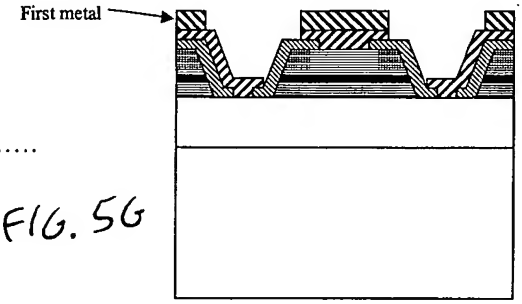
20. Photolith 6: N-metal lift-off mask
21. N-metal stack depostion
22. **N-metal lift-off** .....
23. N-metal sinter

FIG. 5F



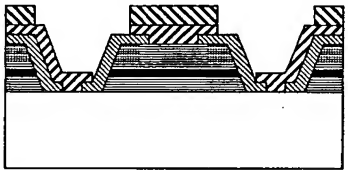
24. Photolith 7: First metal lift-off mask
25. First metal depostion
26. **First metal lift-off** .....
27. On-wafer test

FIG. 5G



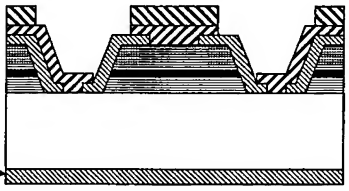
28. Wafer mount (epi side down) on sapphire substrate.
29. **Wafer thinning (lap and polish)** .....

FIG 5H



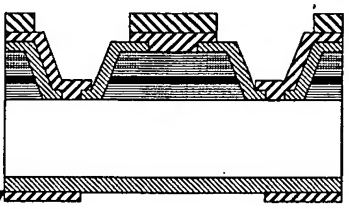
30. **Anti-reflection coating (ARC) deposition** .....

FIG 5I



31. Photolith 8: Aperture metal lift-off mask
32. Aperture metal deposition
33. **Aperture metal lift-off** .....
34. De-mount from sapphire substrate
35. Scribe and break

FIG. 5J



Annotated Marked-Up Drawing
Serial No. 10/735,695 Filed: 12/16/2003
Title: Method of Fabrication of a Support Structure For A Semiconductor Device
Glen Carey et al. Dkt No. 11809/27

~~Fig 6~~

FIG.6A

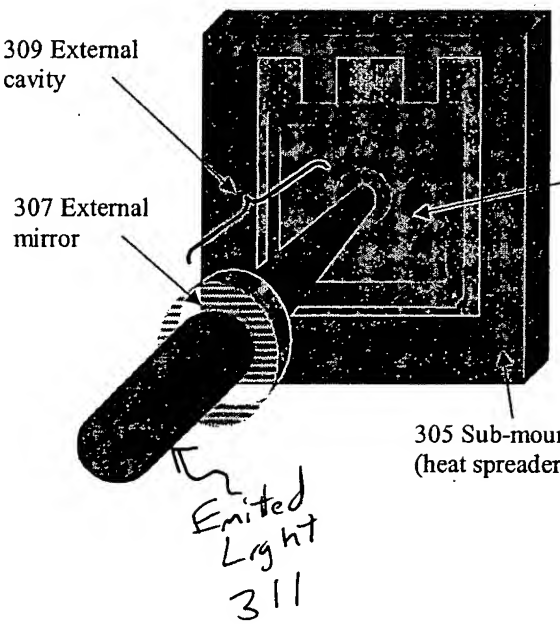


FIG6B